MXD8621C

SPDT Switch for 3G/4G Application

General Description

The MXD8621C is a Single-Pole, Double-Throw (SPDT) LTE/WCDMA/GSM receive switch. Switching is controlled by an integrated GPIO interface with a single control pin.

No external DC blocking capacitors are required as long as no DC voltage is applied on any RF path.

The MXD8621C is provided in a compact 1.1mm x 0.7mm x 0.45mm 6-lead DFN package that meets requirements for board-level assembly.

A functional block diagram and the pin configuration are shown in Figure 1.

Applications

- GSM/WCDMA/LTE receive

Features

- Broadband frequency range: 0.1 to 3.0 GHz
- Low insertion loss: 0.45 dB @ 2.7 GHz
- High isolation: 25 dB up to 2.7 GHz
- P0.1dB 29dBm
- No external DC blocking capacitors required
- Single GPIO control line with VDD voltage regulator:
  V_{CTL}= 1.6 to 3.00 V
  V_{DD}= 2.5 to 3.00 V
- Small, 6-Lead DFN, 400 um pitch (1.1mm x 0.7mmx 0.45 mm) package

Functional Block Diagram and Pin Function

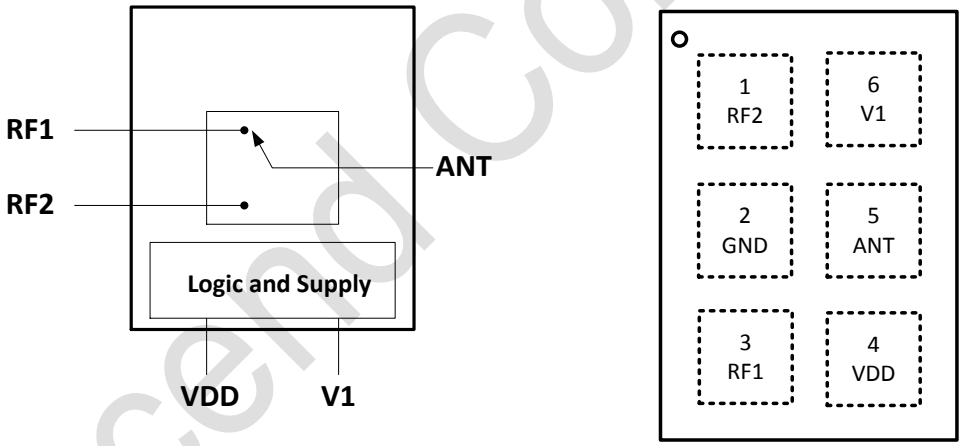


Figure 1 Functional Block Diagram and Pin-out (Top View)

Application Circuit

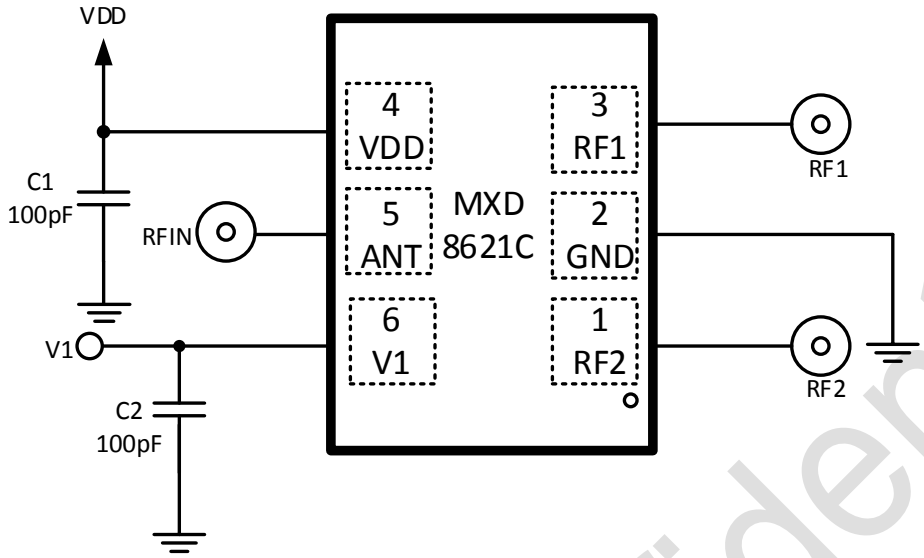


Figure 2 MXD8621C Application Circuit

Table 1. Pin Description

Pin No.	Name	Description	Pin No.	Name	Description
1	RF2	RF I/O. Throw 1 of the switch.	6	V1	Digital
2	GND	Ground	5	ANT	Antenna
3	RF1	RF I/O. Throw 2 of the switch.	4	VDD	Supply

Truth Table

Table 2.

State	Active Path	V1
0	ANT to RF1	0
1	ANT to RF2	1

Note: "1" = 1.6 V to 3.00 V. "0" = 0 V to +0.3 V.

Recommended Operation Range

Table 3.

Parameters	Symbol	Min	Typ	Max	Units
Operation Frequency	f1	0.1	-	3.0	GHz
Power supply	V_{DD}	2.5	2.8	3.0	V
Switch Control Voltage High	V_{CTL_H}	1.6	1.8	3.0	V
Switch Control Voltage Low	V_{CTL_L}	0	0	0.3	V

Specifications

Table 4.Electrical Specifications

Parameter	Symbol	Specification			Units	Test Condition
		Min.	Typical	Max.		
DC Specifications						
Supply voltage	V_{DD}	2.5	2.8	3.0	V	
Control voltage: Low High	 V_{CTL_L} V_{CTL_H}	 0 +1.6	 0 +1.8	 +0.3 +3.0	 V V	
Current on V1 pin	I_{CTL}			5	μA	
Supply current	I_{DD}	20	40	60	μA	V_{DD}= 2.8 V, V1 = V_{CTL_H}
DC supply turn-on/turn-off time	t_{on}			10	μs	Measured from 50% of final V_{DD} supply voltage to 90% of final RF power
RF path switching time	t_{sw}		0.5	2	μs	From one active state to another active state transition, measured from 50% of final control voltage to 90% of final RF power
Supply ripple	V_{PP}			20	mV_{pp}	
RF Specifications						
Insertion loss (RF1 or RF2 to ANT pin)	IL		0.25 0.28 0.35	0.40 0.45 0.50	dB dB dB	700 to 960 MHz 1710 to 2170 MHz 2170 to 2690 MHz
Isolation (ANT to RF1 or RF2)	ISO	32 27 22	35 30 25		dB dB dB	700 to 960 MHz 1710 to 2170 MHz 2170 to 2690 MHz
Input return loss (ANT to RF1 or RF2)	RL	15	20		dB	700 to 2690 MHz
Voltage Standing Wave Ratio, all ports	VSWR		1.25:1	1.5:1	-	Referenced to 50 Ω, 700 to 2690 MHz
0.1dB compression point （from antenna to RF1 and RF2）		28	29		dBm	Tested at 950 MHz
2nd Harmonic (ANT to RF1 or RF2)	2fo		-85		dBm	fo = 700 to 2700 MHz, PIN = +10 dBm
3rd Harmonic (ANT to RF1 or RF2)	3fo		-83		dBm	

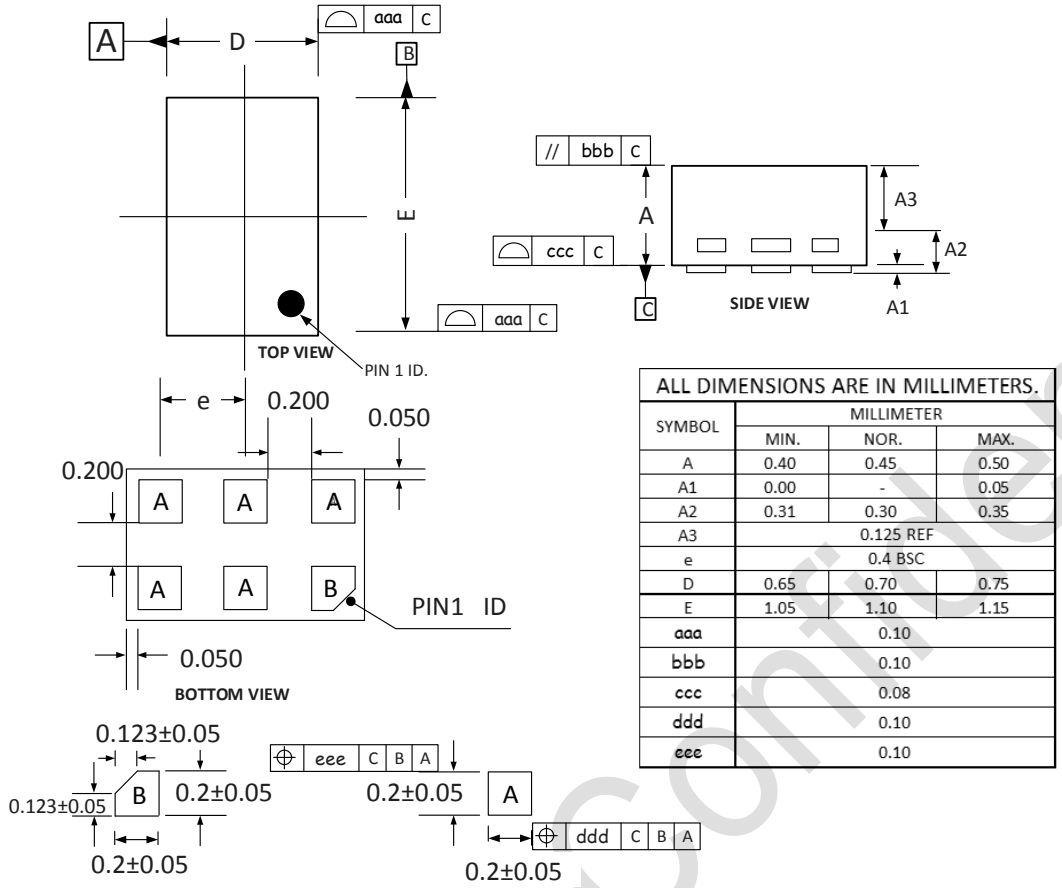
Absolute Maximum Ratings

Table 5. Maximum ratings

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	+2.5	+3.3	V
Digital control voltage	V_{CTL}	0	+3.0	V
RF input power	P_{IN}		+29	dBm
Operating temperature	T_{OP}	–30	+85	℃
Storage temperature	T_{STG}	–55	+150	℃
Electrostatic Discharge Human body model (HBM), Class 1C Machine Model (MM), Class A Charged device model (CDM), Class III	 ESD_HBM ESD_MM ESD_CDM		 1000 100 500	V

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Package Outline Dimension



ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER		
	MIN.	NOR.	MAX.
A	0.40	0.45	0.50
A1	0.00	-	0.05
A2	0.31	0.30	0.35
A3		0.125 REF	
e		0.4 BSC	
D	0.65	0.70	0.75
E	1.05	1.10	1.15
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Figure 3. Package outline dimension

Reflow Chart

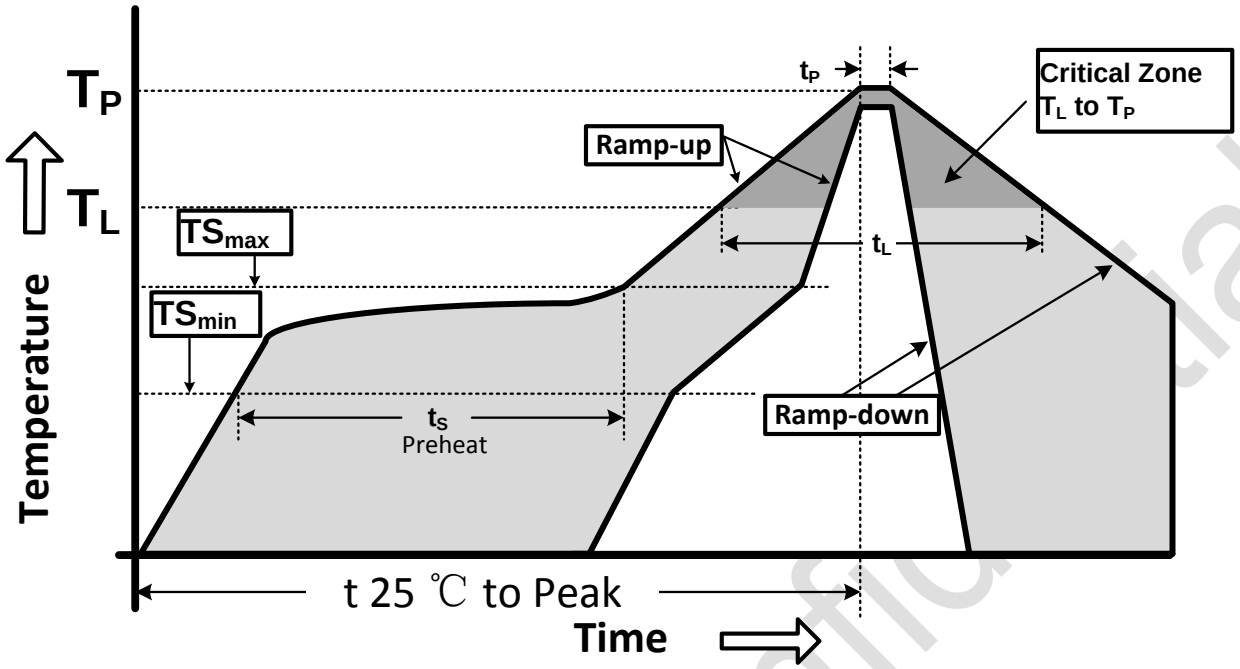


Figure 4. Recommended Lead-Free Reflow Profile

Table 6.

Profile Parameter	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate（TS_{max} to T_p）	3℃/second max.
Preheat temperature（TS_{min} to TS_{max}）	150℃ to 200℃
Preheat time（t_s）	60 - 180 seconds
Time above TL , 217℃（t_L）	60 - 150 seconds
Peak temperature（T_p）	260℃
Time within 5℃ of peak temperature(t_p)	20 - 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.

1.0.1